

WHAT IS CLAIMED IS:

1 1. A digital circuit comprising:
2 a digital processing component capable of operating at
3 a plurality of selected clock frequencies, wherein a maximum
4 delay time of a critical path in said digital processing
5 component is determined by a level of a power supply, VDD, of
6 said digital processing component;
7 an adjustable power supply capable of supplying VDD to
8 said digital processing component; and
9 power supply adjustment circuitry that receives a first
10 selected clock signal and adjusts said level of VDD such that
11 said maximum delay time of said critical path is less than a
12 pulse-width duration between a first clock edge of said first
13 selected clock signal and a second clock edge of said first
14 selected clock signal immediately following said first clock
15 edge.

1 2. The digital circuit as set forth in Claim 1 wherein
2 said power supply adjustment circuitry adjusts said level of VDD
3 such that said maximum delay time is less than said pulse-width
4 duration by not more than a maximum slack time threshold amount.

1 3. The digital circuit as set forth in Claim 2 wherein
2 said power supply adjustment circuitry adjusts said level of VDD
3 such that said maximum delay time is less than said pulse-width
4 duration by not less than a minimum slack time threshold amount.

1 4. The digital circuit as set forth in Claim 3 wherein
2 said power supply adjustment circuitry comprises clock generating
3 circuitry capable of receiving an external reference clock signal
4 and generating therefrom said first selected clock signal.

1 5. The digital circuit as set forth in Claim 4 wherein
2 said power supply adjustment circuitry compares a frequency of
3 said first selected clock signal to a frequency of a previous
4 selected clock signal currently applied to said digital
5 processing component and, in response to a determination that
6 said first selected clock signal frequency is greater than said
7 previous selected clock signal frequency, causes said clock
8 generating circuitry to temporarily disable said first selected
9 clock signal from being applied to said digital processing
10 component.

1 6. The digital circuit as set forth in Claim 5 wherein
2 said power supply adjustment circuitry causes said clock
3 generating circuitry to apply said first selected clock signal to
4 said digital processing component after said power supply
5 adjustment circuitry adjusts said level of VDD such that said
6 maximum delay time is less than said pulse-width duration by not
7 more than a maximum slack time threshold amount and by not less
8 than a minimum slack time threshold amount.

1 7. The digital circuit as set forth in Claim 5 wherein
2 said power supply adjustment circuitry, in response to a
3 determination that said first selected clock signal frequency is
4 less than said previous selected clock signal frequency, causes
5 said clock generating circuitry to apply said first selected
6 clock signal to said digital processing component while said
7 power supply adjustment circuitry adjusts said level of VDD such
8 that said maximum delay time is less than said pulse-width
9 duration by not more than a maximum slack time threshold amount
10 and by not less than a minimum slack time threshold amount.

1 8. The digital circuit as set forth in Claim 7 wherein
2 said power supply adjustment circuitry comprises N delay cells
3 coupled in series, each of said N delay cells having a delay D
4 determined by said level of VDD, wherein said first clock edge is
5 applied to an input of a first delay cell and ripples
6 sequentially through said N delay cells, and wherein said power
7 supply adjustment circuitry: i) monitors outputs of at least a K
8 delay cell and a K+1 delay cell, ii) determines that said first
9 clock edge has reached an output of said K delay cell and has not
10 reached an output of said K+1 delay cell, and iii) generates a
11 control signal capable of adjusting VDD.

1 9. The digital circuit as set forth in Claim 8 wherein
2 said power supply adjustment circuitry determines that said first
3 clock edge has reached said K delay cell output and has not
4 reached said K+1 delay cell output when said second clock edge is
5 applied to said first delay cell input.

1 10. The digital circuit as set forth in Claim 8 wherein a
2 total delay from said first delay cell input to said K delay cell
3 output is greater than said maximum delay time of said critical
4 path.

1 11. The digital circuit as set forth in Claim 8 wherein
2 said power supply adjustment circuitry increases VDD if said
3 first clock edge has not reached said K delay cell output.

1 12. The digital circuit as set forth in Claim 8 wherein
2 said power supply adjustment circuitry decreases VDD if said
3 first clock edge has reached said K+1 delay cell output.

1 13. A method of operating a digital circuit for adjusting a
2 power supply level, VDD, of a digital processing component
3 capable of operating at a plurality of selected clock
4 frequencies, wherein a maximum delay time of a critical path in
5 the digital processing component is determined by a level of a
6 power supply, VDD, of the digital processing component, the
7 method of operating the digital circuit comprising the steps of:

8 supplying VDD to the digital processing component from
9 an adjustable power supply;

10 receiving a first selected clock signal; and

11 adjusting the level of VDD such that the maximum delay
12 time of the critical path is less than a pulse-width duration
13 between a first clock edge of the first selected clock signal and
14 a second clock edge of the first selected clock signal
15 immediately following the first clock edge.

1 14. The method as set forth in Claim 13 wherein the step of
2 adjusting comprises the sub-step of adjusting the level of VDD
3 such that the maximum delay time is less than the pulse-width
4 duration by not more than a maximum slack time threshold amount.

1 15. The method as set forth in Claim 14 wherein the step of
2 adjusting comprises the sub-step of adjusting the level of VDD
3 such that the maximum delay time is less than the pulse-width
4 duration by not less than a minimum slack time threshold amount.

1 16. The method as set forth in Claim 15 wherein the step of
2 receiving the first selected clock signal comprises the sub-step
3 of receiving an external reference clock signal and generating
4 therefrom the first selected clock signal.

1 17. The method as set forth in Claim 16 further comprising
2 the steps of:

3 comparing a frequency of the first selected clock
4 signal to a frequency of a previous selected clock signal
5 currently applied to the digital processing component; and

6 in response to a determination that the first selected
7 clock signal frequency is greater than the previous selected
8 clock signal frequency, temporarily disabling the first selected
9 clock signal from being applied to the digital processing
10 component.

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1 18. The method as set forth in Claim 17 further comprising
2 the step of applying the first selected clock signal to the
3 digital processing component after the power supply adjustment
4 circuitry adjusts the level of VDD such that the maximum delay
5 time is less than the pulse-width duration by not more than a
6 maximum slack time threshold amount and by not less than a
7 minimum slack time threshold amount.

1 19. The method as set forth in Claim 17 further comprising
2 the step, in response to a determination that the first selected
3 clock signal frequency is less than the previous selected clock
4 signal frequency, of apply the first selected clock signal to the
5 digital processing component while the power supply adjustment
6 circuitry adjusts the level of VDD such that the maximum delay
7 time is less than the pulse-width duration by not more than a
8 maximum slack time threshold amount and by not less than a
9 minimum slack time threshold amount.

1 20. The method as set forth in Claim 19 wherein the digital
2 circuit comprises a power supply adjustment circuitry comprising
3 N delay cells coupled in series, each of the N delay cells having
4 a delay D determined by the level of VDD, wherein the first clock
5 edge is applied to an input of a first delay cell and ripples
6 sequentially through the N delay cells, and wherein the method
7 further comprises the steps of:

8 monitoring outputs of at least a K delay cell and a K+1
9 delay cell;

10 determining that the first clock edge has reached an
11 output of the K delay cell and has not reached an output of the
12 K+1 delay cell; and

13 generating a control signal capable of adjusting VDD.

1 21. The method as set forth in Claim 20 further comprising
2 the step of determining that the first clock edge has reached the
3 K delay cell output and has not reached the K+1 delay cell output
4 when the second clock edge is applied to the first delay cell
5 input.

1 22. The method as set forth in Claim 20 wherein a total
2 delay from the first delay cell input to the K delay cell output
3 is greater than the maximum delay time of the critical path.

1 23. The method as set forth in Claim 20 further comprising
2 the step of increasing VDD if the first clock edge has not
3 reached the K delay cell output.

1 24. The method as set forth in Claim 20 further comprising
2 the step of decreasing VDD if the first clock edge has reached
3 the K+1 delay cell output.